

TUNING PROGRAMMABLE LOGIC DEVICES FOR LOW-POWER DESIGN  
IMPLEMENTATION

ABSTRACT

A method of operating a programmable logic device includes the steps of using a full  $V_{DD}$  supply voltage to operate a first set of active blocks of the programmable logic device, and using a reduced supply voltage (e.g.,  $0.9 V_{DD}$ ) to operate a second set of active blocks of the programmable logic device. A timing analysis is performed to determine the maximum available timing slack in each active block. Active blocks having a smaller timing slack are grouped in the first set, and are coupled to receive the full  $V_{DD}$  supply voltage. Active blocks having a larger timing slack are grouped in the second set, and are coupled to receive the reduced  $V_{DD}$  supply voltage. As a result, the active blocks in the second set exhibit reduced power consumption, without adversely affecting the overall speed of the programmable logic device.